MULTI-FINGER LARGE PERIPHERY ALINN/ALN/GAN METAL-OXIDE-SEMICONDUCTOR HETEROSTRUCTURE FIELD EFFECT TRANSISTORS ON SAPPHIRE SUBSTRATE

PRIORITY INFORMATION

The present application is a divisional application of, and claims priority to, U.S. patent application Ser. No. 14/666,768 titled "Multi-Finger Large Periphery AlInN/AlN/GaN Metal-Oxide-Semiconductor Heterostructure Field Effect Transistors on Sapphire Substrate" of Khan, et al. on Mar. 24, 2015, and claims priority to U.S. Provisional Patent Application Ser. No. 61/969,491 titled "Multi-Finger Large Periphery AlInN/AlN/GaN Metal-Oxide-Semiconductor Heterostructure Field Effect Transistors on Sapphire Substrate" of Khan, et al. filed on Mar. 24, 2014; the disclosures of which are incorporated by reference herein.

BACKGROUND

Semiconductor power converters are key building blocks for various applications running the spectrum of powers from a few watts to mega-watts. To date, a majority of the applications use power converters that are based on silicon. For the very high power applications, several groups are now exploring AlGaN based converters as an alternative to silicon, especially when higher operation temperatures are required. Khan, et al. have previously reported the low to the moderate power converter applications by using AlGaN/GaN metal-oxide semiconductor heterostructure field-effect transistors (MOSHFET) based power switch. Since then, rapid progress has been made and several groups including Khan, et al., have reported on kilovolt switching using AlGaN based HEMTs with Schottky gates. In spite of the impressive performance levels, AlGaN/GaN HFET based switching devices suffer from problems such as current collapse, higher ON-state resistance, etc.

Recently, AlInN/GaN heterostructure field-effect transistors (HFETs) have emerged as a strong contender for the realization of high-power and high-frequency electronics for commercial and military applications. They are widely expected to outperform their AlGaN/GaN HEMT counterparts due to the system unique electronic properties such as a high polarization charge and the possibility to grow the materials lattice-matched. HFETs with current densities well above ~2 A/mm have already been demonstrated. These AlInN-based transistors also exhibited outstanding RF characteristics with a current gain cutoff frequency (f_T) reaching 370 GHz for a 30 nm gate length (L_G) device, and a maximum power of 10.3 W/mm with a power-added efficiency of 51% at 10 GHz under dc operation.

Furthermore, a much thinner AlInN barrier (e.g., less than about 12 nm) is usually needed to achieve the same or a higher two-dimensional electron gas (2DEG) charge density in the channel as compared to AlGaN/GaN system. Although such development appears to be very advantageous for device gate scaling below 50 nm for high speed electronics, while still maintaining a sufficiently high aspect ratio to suppress short-channel effects (SCEs), it may also lead to higher gate leakage currents and poor on/off ratios, which have previously been shown to have detrimental effects on the transistors performance and reliability. The metal-insulator-semiconductor (MIS) gate structure wherein a thin dielectric film is deposited on top of the barrier layer prior to gate formation represents a proven method to alleviate this issue along with enabling a larger gate voltage swing. Such insulated gate devices using either SiO_2, Al_2O_3, native oxides, or plasma treatment oxides, as the gate dielectrics have been reported to effectively reduce the gate leakage. However, because of the increased gate-to-channel separation, it is important to limit the insulator thickness to less than 5 nm in order to avoid i) a shift in the MISHFET threshold voltage (VTh) as compared to the Schottky structures, and ii) a degradation of both the extrinsic transconductance as well as the aspect ratio.

Most of the research works on both Schottky gate and insulated gate AlInN/GaN HFETs have been focused on small periphery devices with deep sub-micrometer gate technology that targets primarily high frequency (speed) electronics applications. To the best of our knowledge, there has been only one study of large periphery AlInN-based HFETs for power electronics applications. However, these devices with a 7 nm barrier layer, a 250 nm gate length (L_G) and a 2.5 mm gate width (W_G), delivered a low dc drain current density of 620 mA/mm and exhibited a high leakage current of about 2.5 mA/mm under reverse bias.

SUMMARY

Objects and advantages of the invention will be set forth in part in the following description, or may be obvious from the description, or may be learned through practice of the invention.

MOSHFET devices are generally provided, along with their methods of fabrication. In one embodiment, the MOSHFET device includes a substrate; a multilayer stack on the substrate; a ultra-thin barrier layer on the multilayer stack, wherein the ultra-thin barrier layer has a thickness of about 0.5 nm to about 10 nm; a dielectric, discontinuous thin film layer on portions of the ultra-thin barrier layer, wherein the dielectric, discontinuous thin film layer comprises SiO_2; a plurality of source electrodes and drain electrodes formed directly on the ultra-thin barrier layer in an alternating pattern such that the dielectric, discontinuous thin film layer is positioned between adjacent source electrodes and drain electrodes; a plurality of gate electrodes on the dielectric, discontinuous thin film layer; and a gate interconnect electrically connecting the plurality of gate electrodes.

Other features and aspects of the present invention are discussed in greater detail below.

BRIEF DESCRIPTION OF THE DRAWINGS

A full and enabling disclosure of the present invention, including the best mode thereof to one skilled in the art, is set forth more particularly in the remainder of the specification, which includes reference to the accompanying figures.

FIG. **1** shows a CCD image of a multi-finger (8×250 μm=2 mm gate width) AlInN/GaN MOSHFET on a sapphire substrate fabricated using SiN bridges for source electrodes interconnections.

FIG. **2** shows typical dc output characteristics of 0.25 mm and 2 mm AlInN/GaN MOSHFETs.

FIG. **3** shows the variation of AlInN/GaN MOSHFET drain saturation current with gate width measured in dc and pulsed modes, at V_{GS}=0V.

FIG. **4** shows dc transfer characteristics for AlInN/GaN MOSHFETs with different gate peripheries. The result obtained for 0.25 mm HFET is also shown for comparison.